Claims

[c1] 1. A method of forming a semiconductor device, comprising the steps of:
depositing alternating layers of a first and a second dielectric material, wherein the first and second dielectric materials are selectively etchable at different rates;
forming a first feature within the alternating layers of dielectric material; and
selectively etching the alternating layers of dielectric material to remove at least a portion, but not all, of the first dielectric material in each layer having the first dielectric material and leaving the second dielectric material as essentially unetched.

[c2] 2. The method of claim 1, wherein the first dielectric material comprises a material that etches selectively to the second dielectric material.

[c3] 3. The method of claim 1, wherein the first dielectric material comprises an organic dielectric material and the second dielectric material comprises an inorganic dielectric material.

[c4] 4. The method of claim 1, wherein the first dielectric

material comprises an organic dielectric material selected from the group consisting of: polyarylene ether (SILK™), parylene (N), parylene (F), Teflon, porous polyarylene ether (SILK™), porous parylene (N), porous parylene (F) and porous Teflon, and wherein the second dielectric material comprises an inorganic dielectric material selected from the group consisting of: OSG, SiO_2, FSG, MSQ, porous OSG, porous SiO_2, porous FSG, and porous MSQ.

[c5] 5. The method of claim 1, wherein the first feature comprises a single damascene feature or a dual damascene feature.

[c6] 6. The method of claim 5, wherein the portion of the first dielectric material is removed from a wire trench portion of the dual damascene feature and not removed from a via trench portion of the dual damascene feature.

[c7] 7. The method of claim 1, following the step of selectively etching the alternating layers of dielectric material further comprising:
depositing a conformal liner over a surface of the alternating layers of dielectric material to seal the alternating layers.

[c8] 8. The method of claim 7, wherein the conformal liner

comprises a material selected from the group consisting of: SiCOH, SiO_2, SiN, SiC, and SiCN.

[c9] 9. The method of claim 7, following the step of depositing a conformal liner further comprising:
depositing a layer of conductive material over a surface of the device filling the first feature; and
polishing the surface of the device to remove excess conductive material on the surface of the device, leaving the conductive material within the first feature.

[c10] 10. A method of forming a semiconductor device, comprising the steps of:
depositing alternating layers of a first and a second insulative material;
forming a first feature within the alternating layers of first and a second insulative material; and
forming openings within the layers of first insulative material.

[c11] 11. The method of claim 10, wherein the first insulative material comprises a material that etches selectively to the second insulative material.

[c12] 12. The method of claim 10, wherein the first insulative material comprises an organic dielectric material selected from the group consisting of: polyarylene ether

(SILK™), parylene (N), parylene (F), Teflon, porous polyarylene ether (SILK™), porous parylene (N), porous parylene (F) and porous Teflon, and wherein the second insulative material comprises an inorganic dielectric material selected from the group consisting of: OSG, SiO_2, FSG, MSQ, porous OSG, porous SiO_2, porous FSG, and porous MSQ.

[c13] 13. The method of claim 10, wherein the first feature comprises a single damascene feature or a dual damascene feature.

[c14] 14. The method of claim 13, wherein the first insulative material is removed from a wire trench portion of the dual damascene feature and not a via trench portion.

[c15] 15. The method of claim 10, following the step of forming openings within the layers of first insulative material further comprising:
depositing a conformal liner over a surface of the alternating layers of dielectric material to seal the alternating layers, wherein the conformal liner comprises a material selected from the group consisting of: SiCOH, SiO_2, SiN, SiC, and SiCN.

[c16] 16. A semiconductor device, comprising:
a metal wiring level having alternating layers of a first

dielectric material and a second dielectric material and having a first feature formed within the alternating layers of first and second dielectric material; and
a plurality of openings within the first dielectric material.

[c17] 17. The semiconductor device of claim 16, wherein the first dielectric material comprises a material that etches selectively to the second dielectric material.

[c18] 18. The semiconductor device of claim 16, wherein the first dielectric material comprises an organic dielectric material selected from the group consisting of: polyarylene ether (SILK^{TM}), parylene (N), parylene (F), Teflon, porous polyarylene ether (SILK^{TM}), porous parylene (N), porous parylene (F) and porous Teflon, and wherein the second dielectric material comprises an inorganic dielectric material selected from the group consisting of: OSG, SiO_2, FSG, MSQ, porous OSG, porous SiO_2, porous FSG, and porous MSQ.

[c19] 19. The semiconductor device of claim 18, wherein the first dielectric material is removed from a wire trench portion of the dual damascene feature and not a via trench portion.

[c20] 20. The semiconductor device of claim 16, further comprising:

a conformal liner over a surface of the alternating layers of dielectric material to seal the alternating layers, wherein the conformal liner comprises a material selected from the group consisting of: SiCOH, SiO_2, SiN, SiC, and SiCN.

[c21] 21. The semiconductor device of claim 16, further comprising:
a conductive material within the first feature.

[c22] 22. The semiconductor device of claim 16, further comprising:
a second metal wiring level, having alternating layers of a first dielectric material and a second dielectric material, formed on the metal wiring level having openings within the first dielectric material of the second metal wiring level;
a second feature formed within the alternating layers of first and second dielectric material of the second metal wiring level; and
a plurality of openings within the first dielectric material of the second wiring level.

[c23] 23. A semiconductor device, comprising:
a plurality of alternating first and second insulative layers, wherein the first and second insulative layers have different etch rates;

a first feature formed within the first and second insulative layers;
a plurality of openings within the plurality of first insulative layers formed during a selective etch.

[c24] 24. The semiconductor device of claim 23, wherein the first insulative layer comprises a material that etches selectively to the second insulative layer.

[c25] 25. The semiconductor device of claim 23, wherein the first insulative layer comprises an organic dielectric material and the second insulative layer comprises an inorganic dielectric material.

[c26] 26. The semiconductor device of claim 23, wherein the first insulative layer comprises an organic dielectric material selected from the group consisting of: polyarylene ether (SILK^{TM}), parylene (N), parylene (F), Teflon, porous polyarylene ether (SILK^{TM}), porous parylene (N), porous parylene (F) and porous Teflon, and wherein the second insulative layer comprises an inorganic dielectric material selected from the group consisting of: OSG, SiO_2, FSG, MSQ, porous OSG, porous SiO_2, porous FSG, and porous MSQ.

[c27] 27. The semiconductor device of claim 23, wherein the first feature comprises a single damascene feature or a

dual damascene feature.

[c28] 28. The semiconductor device of claim 27, wherein the openings are within a wire trench portion of the dual damascene feature and not a via trench portion.

[c29] 29. The semiconductor device of claim 23, further comprising:
a conformal liner over a surface of the alternating layers of dielectric material to seal the alternating layers, wherein the conformal liner comprises a material selected from the group consisting of: SiCOH, SiO_2, SiN, SiC, and SiCN.

[c30] 30. The semiconductor device of claim 23, further comprising:
a conductive material within the first feature.